

## ABSTRACT OF THE DISCLOSURE

A programmable logic device (PLD) includes a plurality of logic array blocks (LAB's) connected by a PLD routing architecture. At least one LAB is configured to determine a compression of a plurality of N-bit numbers. The LAB includes look-up table (LUT) logic cells. Each look-up table (LUT) logic cell is configured to input three signals at three respective inputs of that look-up table (LUT) logic cell and to output two signals at two respective outputs of that look-up table logic cell (LUT) that are a sum and carry signal resulting from adding the three input signals. Input lines are configured to receive input signals from the PLD routing architecture that represent the plurality of N-bit numbers and output lines configured to provide output signals to the PLD routing architecture that represent the compression of the plurality of N-bit numbers. LAB internal routing logic connecting the LUT logic cells such that the LUT logic cells collectively process the input signals, received at the input lines, that represent the N-bit numbers to generate the output signals, provided at the output lines, that represent the sum of the N-bit numbers. The LAB internal routing logic is not part of the routing architecture of the PLD. By employing 3:2 compressor LUT logic cells within the LAB, the use of the routing architecture of the PLD is minimized, which contributes to more efficient use of the PLD resources.